REMARKS

Claims 1-30 are pending in the application. The Applicants' attorney has amended claims 1, 2, 10, 20 and 27, and has added new claims 31-33. In view of the following, all previously unallowed claims as amended and newly added claims are in condition for allowance.

Rejection of claims 1-30 Under 35 U.S.C.102(b) As Being Anticipated By US Patent No.5, 661,760 to Patapoutian et al. ("Patapoutian")

Claims 1, 10, 20 and 27

Claims 1, 10, 20 and 27 each recite either a palindromic first group of consecutive bits or palindromic first code symbol, meaning that the first group/code symbol reads the same backward or forward.

For example, referring to paragraph 25 and FIG. 5 of the present application, a first group/code symbol has consecutive bits "0000" representing a logic level "0" and a second group/code symbol has consecutive bits "0011" representing a logic level "1". The first group/code symbol "0000" reads the same backward or forward and is thus palindromic.

Patapoutian, on the other hand, at, *e.g.*, col. 3, Lines 55-58, teaches a scheme that codes a binary one information value (logic level "1") into a symbol "--++" and a binary zero information value (logic level "0") into a symbol "++--". Neither symbol taught by Patapoutian reads the same backward or forward. Accordingly, unlike the claimed first group/code symbol of consecutive bits, neither of Patapoutian's symbols is palindromic.

Claims 2-3, 21-23 and 28-30

Claims 2-3, 21-23 and 28-30 are patentable by virtue of their respective dependencies from claims 1, 10, 20 and 27.

Claims 4, 8, 11, 14, 16 and 24

Claim 4 recites a group of consecutive bits each having a first logic level, the group representing a second logic level. Claims 8 and 24 each recite a first group of four consecutive bits each having a first logic level. Claims 11, 14 and 16 each recite a group of consecutive bits each having a first logic level, the group representing the first logic level.

For example, referring to paragraph 25 and FIG. 5 of the present application, a code symbol has consecutive bits "0000" representing a servo logic level "0". That is, a servo bit having a logic level "0" is coded as four consecutive logic "0" levels.

Patapoutian, on the other hand, at, *e.g.*, col. 3, Lines 55-58, codes a binary one information value (logic level "1") into a symbol consisting of four consecutive bits "--++" and a binary zero information value (logic level "0") into a symbol consisting of four consecutive bits "++--". As can thus be observed, unlike the claimed group of consecutive bits each having only a first logic level, Patapoutian's groups of consecutive bits each include two different logic levels ("+" and "-").

Claims 5-7, 9, 12, 13, 15, 17-19, 25 and 26

Claims 5-7, 9, 12, 13, 15, 17-19, 25 and 26 are patentable by virtue of their respective dependencies from Claims 4, 8, 11, 14, 16 and 24.

CONCLUSION

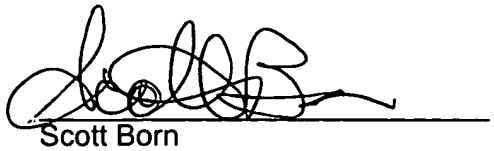
In view of the foregoing, claims 3-9, 11-19, 21-26, and 28-30 as previously pending, claims 1, 2, 10, 20 and 27 as amended, and new claims 31-33 are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes that a telephone conference would expedite prosecution of this application, please telephone the undersigned at 425.455.5575.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,

Dated: February 5, 2004



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